In the Claims

1. [Previously Amended] Integrated circuitry comprising:

a monolithic semiconductive substrate;

a plurality of field effect transistors formed using the monolithic semiconductive substrate and comprising a plurality of electrical contacts including a plurality of gate contacts and a plurality of power contacts including source contacts and drain contacts, wherein the field effect transistors are coupled in parallel with one another to form a power semiconductor switching device and wherein respective ones of the power contacts of the field effect transistors are coupled in common with one another; and

auxiliary circuitry formed using the monolithic semiconductive substrate and configured to couple with at least one of the electrical contacts of the power field effect transistors.

2. [Original] The circuitry of claim 1 wherein the field effect transistors comprise planar field effect transistors.

3. [Original] The circuitry of claim 1 wherein the auxiliary circuitry comprises a gate driver amplifier configured to provide a control signal to the electrical contacts of the field effect transistors comprising the gate contacts.

4. [Original] The circuitry of claim 1 wherein the auxiliary circuitry comprises a power converter controller configured to provide a control signal to the electrical contacts of the field effect transistors comprising the gate contacts.

5. (Previously Amended) The circuitry of claim 1 wherein the gate contacts are coupled in common with one another.

6. [Original] The circuitry of claim 1 wherein the auxiliary circuitry comprises an application specific integrated circuit.

7. [Original] The circuitry of claim 1 wherein the auxiliary circuitry comprises a zero-current switching/timing circuit.

8. [Original] The circuitry of claim 1 wherein the auxiliary circuitry comprises a load protection circuit.

9. [Original] The circuitry of claim 1 wherein the auxiliary circuitry comprises an active snubber circuit.

10. [Original] The circuitry of claim 1 wherein the power semiconductor switching device and the auxiliary circuitry are formed upon a die.

11. [Original] The circuitry of claim 1 wherein the field effect transistors comprise MOSFET devices.

12. [Amended] A method of forming a power transistor comprising:

providing a monolithic semiconductive substrate having a surface;

forming a power field effect transistor comprising a plurality of planar field effect transistors electrically coupled in parallel using the monolithic substrate and having a source contact and a drain contact adjacent to the surface, wherein the power field effect transistor is configured to operably conduct power currents; and

forming auxiliary circuitry using the monolithic semiconductive substrate, the forming comprising coupling the auxiliary circuitry with at least one contact of the power field effect transistor.

13. [Original] The method of claim 12 wherein providing comprises providing the substrate comprising a semiconductor die.

14. Cancel.

15. [Original] The method of claim 12 wherein the forming auxiliary circuitry comprises forming a gate driver amplifier configured to provide a control signal to a gate contact of the power field effect transistor.

16. [Original] The method of claim 12 wherein the forming auxiliary circuitry comprises forming a power converter controller configured to provide a control signal to a gate contact of the power field effect transistor.

17. [Original] The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising application specific integrated circuitry.

18. [Original] The method of claim 12 wherein the formings individually comprise forming the power field effect transistor and the auxiliary circuitry comprising CMOS devices.

19. [Original] The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising zero-current switching\timing circuitry.

20. [Original] The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising active snubber circuitry.

21. [Original] The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising load protection circuitry.

22. [Original] The method of claim 12 wherein the forming the power field effect transistor comprises forming a plurality of MOSFET devices.

23. [Previously Added] The circuitry of claim 1 wherein the commonly-coupled power contacts of the field effect transistors comprise the source contacts commonly-coupled with one another and the drain contacts commonly-coupled with one another.

24. [Previously Added] The circuitry of claim 23 wherein the commonly-coupled source contacts are provided at a first common voltage and the commonly-coupled drain contacts are provided at a second common voltage different than the first voltage.

25. [Previously Added] The circuitry of claim 23 wherein the commonly-coupled source contacts are coupled at a first common node and the commonly-coupled drain contacts are coupled at a second common node.

26. [Previously Added] The circuitry of claim 1 wherein the power semiconductor switching device is configured to operably conduct power currents in excess of 1 Ampere.

27. [Amended] The method of claim 12 wherein the forming the power field effect transistor comprises forming ~~a~~ the plurality of planar field effect transistors including source regions and drain regions adjacent to the surface.

28. [Previously Added] The method of claim 12 wherein the forming the power field effect transistor comprises configuring the power field effect transistor to operably conduct power currents in excess of 1 Ampere.

29. [New] The circuitry of claim 1 wherein the field effect transistors comprise 5,000, or more, transistors coupled in parallel to form the power semiconductor switching device.

30. [New] The circuitry of claim 1 wherein the field effect transistors comprise a common transistor type.

31. [New] The circuitry of claim 1 wherein the field effect transistors comprise only n-channel devices.

32. [New] The circuitry of claim 1 wherein the field effect transistors of the power semiconductor switching device are configured to operably conduct power currents in excess of 20 Amperes.

33. [New] The method of claim 12 wherein the planar field effect transistors comprise 5,000, or more, transistors coupled in parallel to form the power semiconductor switching device.

34. [New] The method of claim 12 wherein the planar field effect transistors comprise a common transistor type.

35. [New] The method of claim 12 wherein the planar field effect transistors comprise only n-channel devices.

36. [New] The method of claim 12 wherein the forming the power field effect transistor comprises configuring the power field effect transistor to operably conduct power currents in excess of 20 Amperes.